Abstract

A test structure of a DRAM array includes a substrate. A transistor is formed on the substrate and has a first region and a second region as source/drain regions thereof. A deep trench capacitor is formed adjacent to the transistor and has a first width. A shallow trench isolation is formed in a top portion of the deep trench capacitor and has a second width. The second width is substantially shorter than the first one. A third region is formed adjacent to the deep trench capacitor. A first contact is formed on the substrate and contacts with the first region. A second contact is formed on the substrate and contacts with the third region.